CLAIMS

What is claimed is:

1. A channel for electrically connecting a source and a drain of a field effect transistor (FET) comprising:

   a channel core coupled to a substrate and defining a top surface spaced from the substrate and opposed sidewall surfaces between the substrate and the top surface, wherein the channel core comprises a first semiconductor material defining a first lattice structure;

   a channel envelope in contact with the opposed sidewall surfaces and the top surface, wherein the channel envelope comprises a second semiconductor material defining a second lattice structure that differs from the first lattice structure; and

   a gate oxide disposed about a surface of the channel envelope that is opposite the channel core.

2. The channel of claim 1 further comprising a gate coupled through the gate oxide to at least two surfaces defined by the channel envelope.

3. The channel of claim 1 wherein at least one of the sidewall surfaces defines a height h_c and the top surface defines a width w_c, and wherein $h_c \geq 3w_c$.

4. The channel of claim 1 wherein the channel is a component of an FET and the FET is a component of a SRAM, and at least one of the sidewall surfaces defines a height h_c that is selected to increase stability of the SRAM.

5. The channel of claim 1 wherein the top surface defines a width w that is selected to maximize one of stretching and of compressing the lattice structure of one of the first and the second semiconductor material.

6. The channel of claim 1 wherein the second semiconductor material substantially covers the two sidewall surfaces and the top surface.

7. The channel of claim 1 wherein one of the first and second semiconductor materials comprises silicon and germanium.

8. In a channel for a field effect transmitter, the improvement comprising:

a channel core defining at least a top and at least one adjoining side surface, and

a channel envelope in contact with the top surface and the at least one side surface, and

a gate oxide disposed on at least two surfaces of the channel envelope, said surfaces of the channel envelope being opposed to the top surface and the at least one side surface,

wherein the channel core comprises a first semiconductor material and the channel envelope comprises a second semiconductor material, and at least one of the first and second semiconductor materials exhibits one of a stretched and a compressed lattice structure.

9. A method for making a FET channel comprising:

providing a substrate and a first semiconductor material overlying the substrate;

defining a first channel core from the first semiconductor material, wherein the channel core defines a top surface spaced from the substrate and opposed first and second sidewalls between the substrate and the top surface;

disposing a layer of second semiconductor material to contact at least two of the top surface, the first sidewall and the second sidewall; and

disposing a gate oxide on at least two exterior surfaces of the channel envelope that are opposed to the at least tow of the top surface, the first sidewall, and the second sidewall.

10. The method of claim 9 wherein the first semiconductor material comprises one of Si or Si_xGe_{1-x} and the second semiconductor material comprises the other of Si or Si_xGe_{1-x}.

11. The method of claim 9 wherein disposing a layer of second semiconductor material comprises masking and etching.

12. The method of claim 11 wherein defining a first channel core comprises defining a first and a second channel core spaced from one another, and disposing a layer of second semiconductor material comprises disposing said layer on the first channel core but not the second channel core.

13. The method of claim 9 wherein disposing a layer of second semiconductor material comprises disposing a carrier wafer with the layer of second semiconductor material over the first channel core, separating at least a portion of said layer from said carrier wafer, and removing said carrier wafer.

14. A method of forming a PFET channel comprising:

providing a substrate and a layer of first semiconductor material overlying the substrate;

defining a trench in said first semiconductor layer that divides said layer into a first section and a second section;

removing a portion of the second section so that a remaining layer of first semiconductor material has a thickness less than a depth of the trench, and a portion of the trench is exposed;

disposing a layer of second semiconductor material over the remaining layer and adjacent to the trench.

15. The method of claim 14 wherein the trench is filled prior to removing a portion of the second section.

16. The method of claim 14 wherein the remaining layer has a thickness less than about 15 nm.

17. The method of claim 14 wherein the second semiconductor material comprises Si_xGe_{1-x}.

18. The method of claim 17 wherein the remaining layer has a thickness less than about 15 nm.

19. A Field Effect Transistor disposed on a substrate comprising:

a source;

a drain;

a fin connecting the source to the drain and defining a channel core and a channel envelope;

a gate coupled through a gate dielectric to at least two surfaces of the fin, wherein the channel core defines at least two surfaces extending from the substrate and comprises a first semiconductor material, and the channel envelope is in contact with the at least two surfaces and comprises a second semiconductor material, and wherein at least one of the first or second semiconductor material exhibits one of a stretched and a compressed lattice structure.

20. An integrated circuit comprising at least one field effect transistor according to claim 19.

21. A field effect transistor (FET) comprising:

a source, a drain, a channel, a gate electrode, and a gate dielectric,

wherein the channel comprises a channel core defining a bottom surface and a top surface spaced from the bottom surface by laterally opposed sidewall surfaces disposed between the bottom surface and the top surface, wherein the channel core comprises a first semiconductor material defining a first lattice structure; the channel further comprising a channel envelope in contact with at least the top surface of the channel core, wherein the channel envelope comprises a second semiconductor material defining a second lattice structure that differs from the first lattice structure,

wherein one of the first and second lattice structures is one of stretched and compressed; and,

wherein the gate electrode is coupled through the gate dielectric to the channel envelope only at a top surface of the channel envelope that is opposed to the top surface of the channel core.

22. The FET of claim 21, wherein the first lattice structure is relaxed relative to the second lattice structure.

23. A field effect transistor (FET) comprising:

a source, a drain, a channel, a gate electrode, and a gate dielectric;

wherein the channel comprises a channel core defining a bottom surface and a top surface spaced from the bottom surface by laterally opposed sidewall surfaces disposed between the bottom surface and the top surface, wherein the channel core comprises a first semiconductor material defining a first lattice structure; the channel further comprising a channel envelope in contact with at least the top surface of the channel core, wherein the channel envelope comprises a second semiconductor material defining a second lattice structure that differs from the first lattice structure; and,

wherein the gate electrode is coupled through the gate dielectric to the channel envelope only at surfaces of the channel envelope that are opposed to the top and bottom surfaces of the channel core.

24. The FET of claim 23, wherein the first lattice structure is relaxed relative to the second lattice structure.

25. A field effect transistor (FET) comprising:

a source, a drain, a channel, a gate electrode, and a gate dielectric;

wherein the channel comprises a channel core defining a bottom surface and a top surface spaced from the bottom surface by laterally opposed sidewall surfaces disposed between the bottom surface and the top surface, wherein the channel core comprises a first semiconductor material defining a first lattice structure; the channel further comprising a channel envelope in contact with at least the top surface and the sidewall surfaces, wherein the channel envelope comprises a second semiconductor material defining a second lattice structure that differs from the first lattice structure; and,

wherein the gate electrode is coupled through the gate dielectric to the channel envelope only at surfaces of the channel envelope that are opposed to the top and sidewall surfaces of the channel core.

26. The FET of claim 25, wherein the first lattice structure is relaxed relative to the second lattice structure.

27. A field effect transistor (FET) attached to a substrate comprising:

a source, a drain, a channel, a gate electrode, and a gate dielectric;

wherein the channel comprises a channel core defining a bottom surface and a top surface spaced from the bottom surface by laterally opposed sidewall surfaces disposed between the bottom surface and the top surface, wherein the channel core comprises a first semiconductor material defining a first lattice structure; the channel further comprising a channel envelope in contact with at least the top surface, wherein the channel envelope comprises a second semiconductor material defining a second lattice structure that differs from the first lattice structure; and,

wherein the gate electrode is coupled through the gate dielectric to the channel envelope at surfaces opposed to the top surface, sidewall surfaces and bottom surface of the channel core.

28. The FET of claim 27, wherein the first lattice structure is relaxed relative to the second lattice structure.

29. A field effect transistor (FET) attached to a substrate comprising:

a source, a drain, a channel, a gate electrode, and a gate dielectric;

wherein the channel comprises a channel core defining a bottom surface and a top surface spaced from the bottom surface by laterally opposed sidewall surfaces disposed between the bottom surface and the top surface, wherein the channel core comprises a first semiconductor material defining a first lattice structure; the channel further comprising a channel envelope in contact with at least the top surface, wherein the channel envelope comprises a second semiconductor material defining a second lattice structure that differs from the first lattice structure; and,

wherein the gate electrode is coupled through the gate dielectric to the channel envelope at surfaces of the channel envelope that are opposed to the top, sidewall, and bottom surfaces of the channel core.

30. The FET of claim 29, wherein the first lattice structure is relaxed relative to the second lattice structure.

31. A static random access memory (SRAM) comprising at least two field effect transistors (FETs), wherein each FET comprises a source, a drain, a gate, a channel defining a height and a width;

wherein each of the at least two FET channels define the same width and each of the two FET channels define a different height.

32. The SRAM of claim 31 wherein the channel of each FET further comprises:

a channel core coupled to a substrate and defining a top surface and spaced from the substrate and opposed sidewall surfaces between the substrate and the top surface, wherein the channel core comprises a first semiconductor material defining a first lattice structure; and

a channel envelope in contact with at least one of the opposed sidewall surfaces and the top surface, wherein the channel envelope comprises a second semiconductor material defining a second lattice structure that differs from the first lattice structure.

33. The SRAM of claim 31wherein, for at least one FET, a ratio of a width of the top surface between the opposed sidewalls to a height of one of the opposed sidewalls promotes stability of the SRAM.

34. A field effect transistor (FET) comprising a source, a drain, a channel defining at least two surfaces defining different planes, a first gate in contact with one of the at least two surfaces through a gate dielectric, and a second gate in contact with the other of the at least two surfaces through a gate dielectric, wherein a voltage applied across at least one of the first or second gates is variable.

35. The FET of claim 34 wherein the channel defines a channel core and a channel envelope, wherein the channel core comprises a first semiconductor material defining a first lattice structure and the channel envelope comprises a second semiconductor material defining a second lattice structure that differs from the first lattice structure, the first and second gate in contact with the channel envelope.